AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (original) A process of manufacturing a substrate for a component used in EUV micro-lithography, comprising the following steps:

providing a base layer consisting of a lithium-aluminosilicate glass ceramic having a coefficient of thermal expansion of no more than 0.1 ppm/K between 0 °C and 50 °C;

polishing said base layer to a surface roughness of one nanometer rms at the most;

applying a first cover layer consisting of silicon onto said base layer by ion beam sputtering up to a layer thickness between 20 nanometers and 200 nanometers;

treating said first cover layer by a method selected from the group formed by ion beam figuring (IBF) and by magneto-rheologic polishing;

applying a second cover layer comprising an organic lacquer up to a layer thickness between 20 and 200 nanometers;

curing said second cover layer;

at least partially removing said second cover layer by a method selected from the group formed by IBF and by magneto-rheologic polishing until a desired surface characteristic is reached.

2. (original) The process of claim 1, further comprising the step of applying a reflective coating onto a top surface of said substrate.

3. (original) The process of claim 1, further comprising the step of structuring said reflective coating.

4. (original) The process of claim 1, wherein said base layer is treated by a method selected from the group formed by IBF and by magneto-rheologic polishing, before said first cover layer is applied.

5. (original) The process of claim 1, wherein said second cover layer is applied by spin coating.

6. (original) A process of manufacturing a substrate for a component used in EUV micro-lithography, comprising the following steps:

providing a base layer consisting of a lithium-aluminosilicate glass ceramic having a coefficient of thermal expansion of no more than 0.1 ppm/K between 0 °C and 50 °C;

polishing said base layer to a surface roughness of one nanometer rms at the most;

applying a first cover layer consisting of silicon onto said base layer by ion beam sputtering up to a layer thickness between 500 nanometers and 2000 nanometers;

treating said first cover layer by a method selected from the group formed by IBF and by magneto-rheologic polishing, until a desired surface characteristic is reached.

7. (original) The process of claim 6, further comprising the step of applying a reflective coating onto a top surface of said substrate.

8. (original) The process of claim 6, further comprising the step of structuring said reflective coating.

9. (original) The process of claim 6, wherein said base layer is treated by a method selected from the group formed by IBF and by magneto-rheologic polishing, before said first cover layer is applied.

10. (cancelled)

11. (currently amended) ~~The process of claim 10,~~ A process of manufacturing a substrate, comprising the following steps:

providing a base layer having a coefficient of thermal expansion of no more than 0.1 ppm/K;

applying a first cover layer of a semiconductor material onto said base layer; and

finishing said first cover layer until a desired surface characteristic is reached;

wherein said first cover layer is treated by a process selected from the group formed by IBF and magneto-rheologic polishing until a shape precision of less than 50 nanometers PV is reached.

12. (cancelled)

13. (cancelled)

14. (cancelled)

15. (cancelled)

16. (cancelled)

17. (cancelled)

18. (cancelled)

19. (cancelled)

20. (cancelled)

21. (currently amended) The process of claim ~~10~~11, further comprising the step of

applying a second cover layer comprising a lacquer onto said first cover layer.

22. (original) The process of claim 21, wherein said second cover layer is applied by spin coating.

23. (original) The process of claim 21, wherein said second cover layer is applied with a layer thickness of 20 nanometers to 500 nanometers.

24. (original) The process of claim 21, wherein said second cover layer is cured and is subsequently at least partially removed.

25. (original) The process of claim 21, wherein said second cover layer is treated by a process selected from the group formed by IBF and magneto-rheologic polishing until a shape precision of less than 50 nanometers PV is reached.

26. (original) The process of claim 21, wherein said first cover layer is treated by a process selected from the group formed by IBF and magneto-rheologic polishing until a surface roughness of less than 0.2 nanometers rms is reached.

27. (currently amended) The process of claim ~~10~~11, wherein said base layer is polished to a surface roughness of less than 1 nanometer rms, before said first cover layer is applied.

28. (currently amended) The process of claim ~~10~~11, wherein said base layer is polished to a surface roughness of less than 0.2 rms, before said first cover layer is applied.

29. (currently amended) The process of claim ~~10~~11, wherein said base layer comprises a material having a coefficient of thermal expansion CTE $\leq$ 0.01 ppm/K in a temperature range of 0 °C to 50 °C.

30. (currently amended) The process of claim ~~10~~11, wherein said base layer comprises a material selected from the group formed by a glass ceramic and a ceramic comprising cordierite.

31. (currently amended) The process of claim ~~10~~11, wherein said base layer comprises a material selected from the group formed by Zerodur®, Zerodur-M®, ULE® and ClearCeram®.

32. (withdrawn) A substrate comprising a base layer and at least one cover layer, wherein said base layer consists of a material having a coefficient of thermal expansion of 0.1 ppm/K at the most, wherein said at least one cover layer consists of a semiconductor material, said substrate comprising a top surface having a shape precision of 50 nanometers PV at the most.

33. (withdrawn) A substrate comprising a base layer and at least one cover layer, wherein said base layer consists of a material having a coefficient of thermal expansion of 0.1 ppm/K at the most, wherein said at least one cover layer consists of a semiconductor material, said substrate comprising a top surface having a surface roughness of 1 nanometer rms at the most.

34. (withdrawn) The substrate of claim 33, wherein the top surface has a surface roughness of less than 0.2 nanometers rms.

35. (withdrawn) The substrate of claim 32, wherein said base layer comprises a material selected from the group formed by Zerodur®, Zerodur-M®, ULE®, ClearCeram® and a ceramic comprising cordierite.

36. (withdrawn) The substrate of claim 33, wherein said base layer comprises a material selected from the group formed by Zerodur®, Zerodur-M®, ULE®, ClearCeram® and a ceramic comprising cordierite.

37. (withdrawn) The substrate of claim 32 being configured as component for the EUV micro-lithography, said component being selected from the group formed by a mask, a structured mask, a mask blank and a mirror.

38. (withdrawn) The substrate of claim 33 being configured as component for the EUV micro-lithography, said component being selected from the group formed by a mask, a structured mask, a mask blank and a mirror.